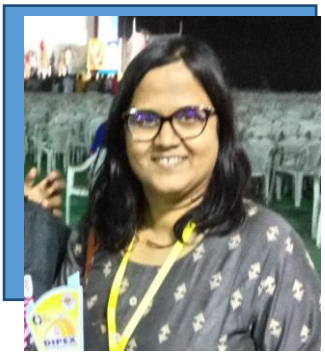
FACULTY PROFILE



NAME	: Ms Swapnali A. Makdey
DESIGNATION	: Assistant Professor
QUALIFICATION	: Pursing PhD at VNIT,Nagpur
EMAIL	: swapnali@frcrce.ac.in
PHONE	: 09769091874
AREA OF INTEREST	: VLSI and Nanotechnology, Neural Network

PROFESSIONAL BACKGROUND : Currently working as Assist. Professor in Department of Artificial Intelligence and Data Science Engineering

EDUCATIONAL DETAILS : Pursuing PhD from VNIT, Nagpur

M.E. ELECTRONICS from FrCRCE, Bandra Mumbai.

ADMINISTRATIVE BACKGROUND :1. CRESCENDO INCHARGE

2. IEDC member 20

3. IEEE –CRCE Branch counselor

4.. IEEE-CRCE Branch Mentor

5. Actively involved in Research Team

PUBLICATIONS : Annexure-I

TRAINING PROGRAMS : Annexure-2

INTERACTION WITH OUTSIDE WORLD :

1. Actively worked as **IEEE-GOLD Chair Bombay Section**
2. Actively worked as **WOMEN Chair IEEE** Bombay section.
3. Actively worked as **Educational Activity Chair IEEE Bombay Section.**
4. Currently worked as **IEEE Executive Committee member of IEEE Bombay section**

PROFESSIONAL AFFILIATIONS : ISTE Membership

IEEE Membership

OTHERS DETAILS

1. Received second prize at DIPEX2018 for project " Rpiscope: an effective Tool for famer s"

2. Mentored the project titled," Rpi-scope An effective tool for famers demonstrated at regional finals of e-yantra idea competition (eYIC-2019)

3 Recognized as best IEEE branch counselor in IEEE BOMBAY section

4. IEEE-CRCE website was awarded the Third prize at IEEE Region 10 &Fourth prize at international level, during my tenure as IEEE Branch counselor

5. Worked as judge in MP-Proex 2009, National Level Project Exhibition, Paper Presentation and Technical Quiz contest.

6. Received consolation prize in 'ELECTRAMA' 99 held at mumbai for "PC based Green house automation

Annexure: -1

PUBLICATIONS

[1] Sharda Narawade, Swapnali Makdey, "Study on Performance of 22nm Single Gate and Multi-Gate MOSFET" IJSER 2347-3878 ,Octomber 2016

[2]Tushar Surwadkar, Swapnali Makdey "Upgrading the performance of VLSI circuits using FinFETs" International Journal of Engineering Trends and Technology (IJETT) , Volume 14 Number 4,Aug 2014, ISSN: 2231-5381 Page 179-184.IJETT-V14P236

[3] Dattaprasad Madur , Dr. Deepak Bhoir, .Swapnali Makdey,"Three Dimensional integration of CMOS" International Journal of Electronics and Communication Engineering and Technology (IJECET 2014-15), Volume 5, Issue 11, November (2014), pp. 01-05

[4] Akhil Ulhas Masurkar, Swapnali Mahadik "Optimization Of Subthreshold Slope In Submicron MOSFET's For Switching Applications," Advances in Computing, Communication, and Control,Spinger, ICAC32013,CCIS361,PP712-720,2013

[5] Akhil Ulhas Masurkar, Swapnali Mahadik "Optimization Of Subthreshold Slope In Submicron MOSFET's for Switching Applications,"INDICON 2012, pp1200-1204

[6] Akhil masurkar Swapnali mahadik " Optimized Estimation of Drain to source currents in submicron MOSFETs using MATLAB|" in the procedding of ISCI 2012

[7] Akhil masurkar ,Swapnali mahadik " Mitigating Techniques to reduce Sub-threshold currents in submicron MOSFETs" in the procedding of "International Journal of scientific & engineering Research volume 3 issue 5 May 2012

[8] Swapnali mahadik , Prof. D. V. Bhoir, K Narayanan " Access control System using fingerprint Recognition" in ACM Digital library, ICAC3 09 at Fr.C.R.C.E

[9] Swapnali mahadik, Prof. D. V. Bhoir "Fingerprint Recognition" in National conference on signal processing &Automation organized by D.Y.Patil, Pune 2007

[10] Swapnali Makdey, "2D material based varactor," International Conference on Nanoscience and Nanotechnology Jan. 28-30th 2019

[11] Swapnali Makdey, Jayen Modi, Deepak Bhoir, "Understanding Semiconductor Construction & Fabrication with 3-D Modeling" OBE symposium at DY Patil University on Saturday, 8th December 2018.

[12] Swapnali Makdey "RpiScope:An Effective tool for farmers" in International conference on recent innovations in electrical ,electronics and communication engineering on july 27th -28th 2018 with IEEE Xplore ISBN:978-1-5386-5994-6"

[13] Makdey, S., Patrikar, R. and Hashmi, M.F., 2020. Modeling and implementation of spin diode based on two dimensional materials using Monte Carlo sampling method. Circuit World, 47(4), pp.357-367.

Annexure: -2

1. Participated in the two weeks ISTE-AICTE short term training programme on **"Mobilisation of financial resources in technical Institutes by Industry Institute Interaction"** organized by ISTE chapter of M.G.M.'s College of Engg. Nanded. (M.S.) Jan 07th to 18th 2002.

2. Participated in AICTE – ISTE " **A winter school on E-Commerce and internet"** from 23 rd December 2002 to 4th January 2003 held at the Dept of computer science and Engg.of T.K.I.E.T. Warnanagar as approved by AICTE – ISTE.

3. Participated in the two weeks ISTE-AICTE short term training two weeks ISTE-AICTE short term training "DIGITAL **CONTROL AND ROBOTICS"** organized by C.O.E.P. Pune

4. Participated in the two weeks ISTE-AICTE short term training two weeks ISTE-AICTE short term training "DIGITAL **CONTROL AND ROBOTICS"** organized by C.O.E.P. Pune.

5. Participated in ISTE-AICTE a one-week short-term training programme on **"Microcontroller and embedded Programming"** conducted from 23rd to 28th feb 2004 at K.J.S.I.E, sion.

6. Participated in the two days workshop on **"Hands on Experience InVLSI and embedded system design"**, approved by ISTE. and organized by L.T.C.E. Navi Mumbai during 16th march to 17th march 2005.

7. Participated the Seminar on **"MECHATRONICS"**
   (feb 04 and 05, 2005) organized by F.R.C.R.C.E. Bandra.

8. Participated the Seminar on **"POWER ELECTRONICS"**
   (18th march 2006) organized by F.R.C.R.C.E. Bandra.

9. Participated in the two weeks ISTE-AICTE short term training programme on **"RECENT TRENDS IN DIGITAL IMAGE PROCESSING"** 31 DEC 2007 to 11 Jan 2008 organized by DBIT Kurla Mumbai.

10. Participated in "Insight09" organized **by Infosys** , Pune on 12th &13th May 2009

11. Participated in **"Mission -10X"** workshop organized by **WIPRO** at Fr.crce,23rd -27th Nov 2009

12. Participated in the one day short term training programme on **"Semiconductor Device Modeling using Visual TCAD&GENIUS 3D",** organized by SPIT, Mumbai

13. Participated in the two weeks short term training programme on **"Faculty Development Program in Entrepreneurship "** 12th march 2013 to 23rd march 2013 organized by DST

14. Participated in the one week short term training programme on **"Semiconductor Technology & Manufacturing"** December 10th -15th 2013 organized by CEP IIT Bombay

15. Participated in the one week short term training programme on **"INUP Hands on training Workshop on fabrication of MEMS sensor"** December 10th -15th organized by INUP IIT Bombay

16. Participated in the two weeks short term training programme on **"Electronic System Design from Device to applications " 4th- 15th** May 2015 organized by SPIT Mumbai

17. Participated in the one week short term training programme on **"Analog CMOS VLSI design""** December 7th -12th December 2015 organized by SPIT Mumbai

18. Participated in the one week short term training programme on **"MEMS Devices""** December 16th -21st November 2015 organized by SPIT Mumbai

19. Participated in the one week short term training programme on **" MEMS &Nanoelectronics"** 11-15th April 2016 organized by VNIT Nagpur

20. Participated in the two weeks short term training programme on Hands on Training on "**Multiscale Simulation in Advanced Materials Science & Technology (HTMSAMST-2016**)" during14-24 July 2016, SVNIT, Surat

21. Successfully completed faculty development program on **LaTeX** organized at Sanjay Ghodawat University in association with theSpoken Tutorial Project, IIT Bombay.

22. Participated in hands-on workshop on **Artificial Intelligence and Deep learning** held at Bennett University, Greater Noida