Lesson Plan

S.E. (COMPS) DIV-B (Semester III)

Subject: Digital Logic & Computer Organization and Architecture

Subject code: CSC304

Teacher-in-charge: Prof. Heenakausar Pendhari

Academic Term: July – October 2022

Module		Detailed Content	Hours
1		**Computer Fundamentals**	**5**
	1.1	Introduction to Number System and Codes	
	1.2	Number Systems: Binary, Octal, Decimal, Hexadecimal,	
	1.3	Codes: Grey, BCD, Excess-3, ASCII, Boolean Algebra.	
	1.4	Logic Gates: AND, OR, NOT, NAND, NOR, EX-OR	
	1.5	Overview of computer organization and architecture.	
	1.6	Basic Organization of Computer and Block Level functional Units, Von-Neumann Model.	
2		**Data Representation and Arithmetic algorithms**	**8**
	2.1	Binary Arithmetic: Addition, Subtraction, Multiplication, Division using Sign Magnitude, 1's and 2's compliment, BCD and Hex Arithmetic Operation.	
	2.2	Booths Multiplication Algorithm, Restoring and Non-restoring DivisionAlgorithm.	
	2.3	IEEE-754 Floating point Representation.	
3		**Processor Organization and Architecture**	**6**
	3.1	Introduction: Half adder, Full adder, MUX, DMUX, Encoder, Decoder(IClevel).	
	3.2	Introduction to Flip Flop: SR, JK, D, T (Truth table).	
	3.3	Register Organization, Instruction Formats, Addressing modes, InstructionCycle, Interpretation and sequencing.	
4		**Control Unit Design**	**6**
	4.1	Hardwired Control Unit: State Table Method, Delay Element Methods.	
	4.2	Microprogrammed Control Unit: Micro Instruction-Format, Sequencing andexecution, Micro operations, Examples of microprograms.	
5		**Memory Organization**	**6**
	5.1	Introduction and characteristics of memory, Types of RAM and ROM, Memory Hierarchy, 2-level Memory Characteristic,	
	5.2	Cache Memory: Concept, locality of reference, Design problems based on	

Course Objectives:

1. To have the rough understanding of the basic structure and operation of basic digital circuits and digital computer.
2. To discuss in detail arithmetic operations in digital system.
3. To discuss generation of control signals and different ways of communication with I/O devices.
4. To study the hierarchical memory and principles of advanced computing.

Course Outcomes:

Upon completion of this course students will be able to:

CSC304.1: To learn different number systems and basic structure of computer system.
CSC304.2: To demonstrate the arithmetic algorithms.
CSC304.3: To explain the basic concepts of digital components and processor organization.
CSC304.4: To explain the generation of control signals of computer.
CSC304.5: To demonstrate the memory organization.
CSC304.6: To describe the concepts of parallel processing and different Buses.

CO-PO-PSO Mapping:

	PO1 (Engg Know)	PO2	PO3 (Design)	PO4	PO5 (tools)	PO6 (engg Soci)	PO7 (Env)	PO8 (Eth)	PO9 (ind Team)	PO10 (com.)	PO11 (PM)	PO12 (life Long)	PSO1	PSO2
CSC304.1	2													
CSC304.2	2	1												
CSC304.3	2		1											
CSC304.4	2													
CSC304.5	2	1												
CSC304.6	2													
Course To PO	2	1	1											

Justification of PO to CO mapping

Course Outcome	Competency	Performance Indicator
CSC304.1	1.1 Demonstrate competence in mathematical modelling	1.1.1 Apply the knowledge of discrete structures, linear algebra, statistics and numerical techniques to solve problems
	1.3 Demonstrate competence in engineering fundamentals	1.3.1 Apply engineering fundamentals

	3.2 Demonstrate an ability to generate a diverse set of alternative design solutions	3.2.1 Able to explore design alternatives. 3.2.2 Able to produce a variety of potential design solutions suited to meet functional requirements.
CSC304.2	1.3 Demonstrate competence in engineering fundamentals	1.3.1 Apply engineering fundamentals
	1.4 Demonstrate competence in specialized engineering knowledge to the program	1.4.1 Apply theory and principles of computer science and engineering to solve an engineering problem
	2.4 Demonstrate an ability to execute a solution process and analyze results	2.4.1 Applies engineering mathematics to implement the solution. .
CSC304.3	1.3 Demonstrate competence in engineering fundamentals	1.3.1 Apply engineering fundamentals
	1.4 Demonstrate competence in specialized engineering knowledge to the program	1.4.1 Apply theory and principles of computer science and engineering to solve an engineering problem
	3.2 Demonstrate an ability to generate a diverse set of alternative design solutions	3.2.1 Able to explore design alternatives.
CSC304.4	1.3 Demonstrate competence in engineering fundamentals	1.3.1 Apply engineering fundamentals
	1.4 Demonstrate competence in specialized engineering knowledge to the program	1.4.1 Apply theory and principles of computer science and engineering to solve an engineering problem
CSC304.5	1.3 Demonstrate competence in engineering fundamentals	1.3.1 Apply engineering fundamentals
	1.4 Demonstrate competence in specialized engineering knowledge to the program	1.4.1 Apply theory and principles of computer science and engineering to solve an engineering problem
	2.3 Demonstrate an ability to formulate and interpret a model	2.3.1 Able to apply computer engineering principles to formulate modules of a system with required applicability and performance.
CSC304.6	1.3 Demonstrate competence in engineering fundamentals	1.3.1 Apply engineering fundamentals
	1.4 Demonstrate competence in specialized engineering knowledge to the program	1.4.1 Apply theory and principles of computer science and engineering to solve an engineering problem

Justification of PSO to CO mapping

No PSO maps with the COs

CO Assessment Tools:

Course Outcomes	***Indirect Method (20%)***								
	Unit Tests		Assignments		Quizzes			End Sem Exam	Course exit survey
	1	2	1	2	1	2	3		
CSC304.1	20%	--	20%	--	10%	--	----	50%	100%
CSC304.2	----	20%	20%	--	10%	--	-----	50%	100%
CSC304.3	20%	----	--	20%	10%	--	----	50%	100%
CSC304.4	--	20%	--	20%	--	10%	-----	50%	100%
CSC304.5	--	20%	--	20%	--		10%	50%	100%
CSC304.6	--	----	--	25%	--	25%	-----	50%	100%

CO calculation= (0.8 *Direct method + 0.2*Indirect method)

Rubrics for assessing Course Outcome with each assessment tool:

Assignment:

Rubrics for Assignment Grading:

Indicator				
Timeline (2)		More than one session late (0)	One sessions late (1)	On time (2)
Level of content (4)	Just Managed (1)	Major points are addressed minimally (2)	Only major topics are covered(3)	Most major and some minor criteria are included. Information is Adequate (4)
Reading and Understanding (4)	Just Managed (1)	Superficial at most (2)	Understood concepts but no related topics (3)	Understood concepts and related topics (4)

Curriculum Gap identified: (with action plan)

SOP and POS concepts , K-Maps. Extra lectures conducted.

Content beyond syllabus:

Practical on : Design of 3-bit Counter using JK Flipflops

Modes of content delivery

Modes of Delivery	Brief description of content delivered
Class room lecture	1. Computer Fundamentals 2. Data Representation and Arithmetic algorithms 3. Processor Organization and Architecture 4. Control Unit Design 5. Memory Organization 6. Principles of Advanced Processor and Buses
Assignments	Assignment 1: based on Computer Fundamentals Assignment 2: based on Data Representation and Arithmetic algorithms Assignment3: 3,4,5,6
Flip Classroom Activity	Module 5: Memory Organization
Quizzes	Quiz 1: on Module 1,2,3 Quiz 2: on 4,6 Quiz3: on 5

Textbooks:	
1	R. P. Jain, "Modern Digital Electronic", McGraw-Hill Publication, 4thEdition.
2	William Stalling, "Computer Organization and Architecture: Designing and Performance",Pearson Publication 10TH Edition.
3	John P Hayes, "Computer Architecture and Organization", McGraw-Hill Publication, 3RDEdition.
4	Dr. M. Usha and T. S. Shrikanth, "Computer system Architecture and Organization", Wiley publication.
References:	
1	Andrew S. Tanenbaum, "Structured Computer Organization", Pearson Publication.
2	B. Govindarajalu, "Computer Architecture and Organization", McGraw-Hill Publication.
3	Malvino, "Digital computer Electronics", McGraw-Hill Publication, 3rdEdition.
4	Smruti Ranjan Sarangi, "Computer Organization and Architecture", McGraw-Hill Publication.

Lesson Plan

CLASS	SE Computer Engineering (B), Semester III
Academic Term	July- October 2022
Subject	**Digital Logic & Computer Organization and Architecture (CSC304)**

Periods (Hours) per week	***Lecture***	***3***	
	Practical		
	Tutorial		
Evaluation System		***Hours***	***Marks***
	Theory examination	3	80
	Internal Assessment	--	20
	Practical Examination	--	--
	Oral Examination	--	--
	Term work	--	--
	Total	--	100

Time Table	***Day***	***Time***
	Monday	12-1pm
	Wednesday	12-1pm
	Thursday	12-1pm

Course Content and Lesson plan

Week	**Lecture**	**Date**		**Topic**	
		Planned	**Actual**		**Remarks**
Module 1: Computer Fundamentals					
1	1	25-07-22	25-07-22	Introduction to subject . Discussion on different Course outcomes Logic Gates: AND,OR,NOT,NAND,NOR,EX-OR	https://www.youtube.com/watch?v=SW2Bwc17_wA
	2	26-07-22	26-07-22	Derivation of basic gates from universal gates	
	3	29-07-22	29-07-22	Codes: Grey, BCD, Excess-3	
	4	1-08-22	1-08-22	ASCII, Boolean Algebra.	
	5	3-08-22	3-08-22	Problems on Boolean Algebra	
	6	4-08-22	4-08-22	SOP and POS form of logical equation Introduction to K-map	Content beyond Syllabus
	7		8-08-22	2 variable 4-variable K-map, problems on K-Map	Content beyond Syllabus

Module 3: Processor Organization and Architecture					
2	8	8-08-22	10-08-22	Half adder Full adder design using K-map	
	9	10-08-22	11-08-22	Subtractor : Full, Half using K-map. Introduction to Multiplexer	Assignment-1
	10	11-08-22	17-08-22	Multiplexer tree, Design problems on Multiplexer,	
3	11	17-08-22	18-08-22	Realization of logical equation using Multiplexer, IC 74151	
	8	18-08-22	18-08-22	Introduction to Demultiplexer, Decoder,	
	9	22-08-22	24-08-22	Design Problems on Decoder IC 74138	
	12	24-8-22	25-08-22	Introduction to Flip Flop: SR, JK, D, T (Truth table)	
	13	25-08-22	29-08-22	Introduction to Flip Flop: SR, JK, D, T (Truth table)	
	14		8-09-22	Design of 2bit and 3bit counter using JK, T flipflop.	Content beyond Syllabus
Module 1: Computer Fundamentals					
	15	29-8-22	12-09-22	Introduction to Number system Number Systems: Binary, Octal, Hexadecimal,	
4	16	8-09-22	14-09-22	Number Systems: Binary, Octal, Hexadecimal	
Module 2: Data Representation and Arithmetic algorithms.					
5	17	12-9-22	15-09-22	Binary Arithmetic: Addition, Subtraction, using Sign Magnitude, 1's and 2's compliment, Operation.	
	18	14-9-22	19-9-22	BCD and Hex Arithmetic , problem based on it.	
	19	15-9-22	21-9-22	Multiplication, Booths Multiplication Algorithm.	
	20	19-9-22	22-9-22	Booths Multiplication Algorithm	
	21	21-9-22	26-9-22	Division, Restoring and Non-restoring DivisionAlgorithm.	
	22	22-9-22	28-9-22	Division, Restoring and Non-restoring DivisionAlgorithm.	Assignment-2
	***Module 3:* Processor Organization and Architecture**				
	23	26-9-22	29-9-22	Register Organization	

	24	28-9-22	3-10-22	Instruction Formats Addressing modes	
7	25	29-10-22	4-10-22	InstructionCycle, Interpretation and	
	***Module 4:* Control Unit Design**				
	26	3-10-22	4-10-22	Hardwired Control Unit: State Table Method,	
8	27	6-10-22	6-10-22	Hardwired Control Unit: Delay Element Methods	
	28	10-10-22	6-10-22	Microprogrammed Control Unit:	
	29	12-10-22	8-10-22	Instruction-Format, Sequencing and execution	
9	30	13-10-22	7-10-22	Micro operations, Examples of microprograms.	Assignment-3
10	***Module 5:* Memory Organization**				
	31		7-10-22	Introduction and characteristics of memory, Types of RAM and ROM,	Flip classroom Activity
	32		10-10-22	MemoryHierarchy, 2-level Memory Characteristic,	
	33		11-10-22	Cache Memory: Concept, locality of reference	
11	34		12-10-22	Cache Mapping techniques: Fully Associative	
	35		13-10-22	Cache Mapping techniques:Direct	
	36		13-10-22	Cache Mapping techniques: Set Associative	
	37		20-10-22	Cache coherence and write policies. Interleaved and Associative Memory.	Online
13	***Module 6:* Principles of Advanced Processor and Buses**				
	38		20-10-22	Basic Pipelined Data path and control	Online
	39		21-10-22	data dependencies, data hazards	Online
14	40		21-10-22	Branch hazards, delayed branch	Online
15	41		22-10-22	Branch prediction	Online
	42		27-10-22	Introduction to buses: ISA, PCI, USB. Bus	Nptel video
Tota	42				

***** Note Planned extra lectures to complete the syllabus**

Video Links:

You tube: Video1 Transistors and Boolean logic https://www.youtube.com/watch?v=SW2Bwc17_wA

You tube :Video2 Animation RS Flip Flop https://www.youtube.com/watch?v=--pv3MZMoo0

You tube :Video3 Introduction to counter https://www.youtube.com/watch?v=iaIu5SYmWVM

Submitted By	**Approved By**
Prof. Heenakausar Pendhari	ii) Dr. Sujata Deshmukh Sign:
Sign:	ii) Dr. B. S. Daga Sign:
	iii) Prof. Merly Thomas Sign:
	iv) Prof. Monica Khanore
	v) Prof. Roshni Padate Sign:
	vi) Prof. Kalpana Deorukhkar Sign:
Date of Submission:	**Date of Approval:** 26/08/2022
Remarks by DQAC (if any)	