Lesson Plan

Branch: Computer Engineering
Semester: IV **Year: 2022-23**

Course Title: Microprocessor (CSC405)	SEE: 3 Hours – Theory
Total Contact Hours: 36 Hours	Duration of SEE: 3 Hrs
SEE Marks: 80 (Theory) + 20 (IA)	
Lesson Plan Author: Prof. Parshvi Shah	Date: 28/01/2023
Checked By:	Date:

Prerequisites: Digital Logic and Computer Architecture

Syllabus

Module	Detailed Contents		Hours
1	**The Intel Microprocessors 8086 Architecture**		8
	1.1	8086CPU Architecture,	
	1.2	Programmer's Model	
	1.3	Functional Pin Diagram	
	1.4	Memory Segmentation	
	1.5	Banking in 8086	
	1.6	Demultiplexing of Address/Data bus	
	1.7	Functioning of 8086 in Minimum mode and Maximum mode	
	1.8	Timing diagrams for Read and Write operations in minimum and maximum mode	
	1.9	Interrupt structure and its servicing	
2	**Instruction Set and Programming**		**6**
	2.1	Addressing Modes	
	2.2	Instruction set-Data Transfer Instructions, String Instructions, Logical Instructions, Arithmetic Instructions, Transfer of Control Instructions, Processor Control Instructions	
	2.3	Assembler Directives and Assembly Language Programming, Macros, Procedures	
3	**Memory and Peripherals interfacing**		**8**
	3.1	Memory Interfacing - RAM and ROM Decoding Techniques – Partial and Absolute	
	3.2	8255-PPI-Block diagram, CWR, operating modes, interfacing with 8086.	
	3.3	8257-DMAC-Block diagram, DMA operations and transfer modes.	
	3.4	Programmable Interrupt Controller 8259-Block Diagram, Interfacing the 8259 in single and cascaded mode.	
4	**Intel 80386DX Processor**		**7**
	4.1	Architecture of 80386 microprocessor	
	4.2	80386 registers – General purpose Registers, EFLAGS and Control registers	

Course Outcomes (CO):

On successful completion of course learner will be able to:

CSC405.1 Describe core concepts of 8086 microprocessors. [Remembering-B1, Understanding-B2]
CSC405.2: Apply the instructions of 8086 and write assembly language programs.
[Understanding-B2& Apply-B3]
CSC405.3: Design 8086 based system using memory and peripheral chips. [Apply-B3; Create -B6]
CSC405.4: Appraise the architecture of advanced processor. [RememberingB1&UnderstandingB2]

CO-PO Mapping:(BL – Blooms Taxonomy, C – Competency, PI – Performance Indicator)

CO	BL	C	PI	PO	Mapping
CSC405.1	1,2	1.3	1.3.1	PO1	1
CSC405.2	2,3	1.3	1.3.1	PO1	1
CSC405.3	3,6	1.3	1.3.1	PO1	1
		2.3	2.3.1	PO2	1
		3.2	3.2.1	PO3	1
CSC405.4	2,3	1.3	1.3.1	PO1	1

Include competencies and PIs

CO-PO-PSO Mapping:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CSC405.1	1											
CSC405.2	1	1										
CSC405.3	1	1	1									
CSC405.4	1											

Note: None of the PSOs Map to the CSC405

CO Measurement Weightages for Tools:

	Test1	Test2	Assign1	Assign 2	Assign-3	Quiz 1	Quiz 2	SEE (T)	Course Exit Survey

CSC405.1	20%		10%			10%		60%	100%
CSC405.2	20%			10%		10%		60%	100%
CSC405.3	10%	10%			20%			60%	100%
CSC405.4		20%					20%	60%	100%

Attainment:

CO CSC405.1:
Direct Method

$A_{csc405.1D}$ = 0.2*test1+ 0.1* Assignment1+ 0.1*quiz1 + 0.6 * SEE_Theory

Final Attainment: $A_{csc405.1} = 0.8 * A_{csc405.1D} + 0.2 * A_{csc405.1I}$

CO CSC405.2:
Direct Method

$A_{csc405.2D}$ = 0.2*test1+ 0.1* Assignment2+ 0.1*quiz1 + 0.6 * SEE_Theory

Final Attainment: $A_{csc405.2} = 0.8 * A_{csc405.2D} + 0.2 * A_{csc405.2I}$

CO CSC405.3:
Direct Method

$A_{csc405.3D}$ = 0.1*test1+0.1*test2+ 0.2* Assignment3 + 0.6 * SEE_Theory

Final Attainment: $A_{csc405.3} = 0.8 * A_{csc405.3D} + 0.2 * A_{csc405.3I}$

CO CSC405.4:
Direct Method

$A_{csc405.4D}$ = 0.2*test2 + 0.2*quiz1 + 0.6 * SEE_Theory

Final Attainment: $A_{csc405.4} = 0.8 * A_{csc405.4D} + 0.2 * A_{csc405.4I}$

Lecture Plan:

Module	Contents	Hours	Planned date	Actual date	Content Delivery Method	Remark
1	**The Intel Microprocessors 8086 Architecture**					
	Introduction, 8086CPU Architecture	**1**	**09/01/2023**		**ppts**	
	8086CPU Architecture	**1**	**11/01/2023**		**ppts**	
	Flag Register, Functional Pin Diagram	**1**	**13/01/2023**		**ppts**	
	Memory Segmentation, Introduction to Banking in 8086	**1**	**16/01/2023**		**ppts**	
	Functioning of 8086 in Minimum mode	**1**	**18/01/2023**		**ppts**	

	Functioning of 8086 in Maximum mode	**1**	**20/01/2023**		**ppts**	
	Demultiplexing of Address/Data bus, Timing diagrams for Read and Write operations in minimum	**1**	**23/01/2023**		**ppts**	
					ppts	
	Timing diagrams for Read and Write operation in maximum mode	**1**	**24/01/2023**		**ppts**	
	Interrupt structure and its servicing	**1**	**25/01/2023**		**ppts**	
	Interrupt structure and its servicing	**1**	**30/01/2023**		**ppts**	**Assignment 1**
2	**Instruction Set and Programming**					
	Addressing Modes	**1**	**31/01/2023**		**ppts**	
	Addressing Modes	**1**	**01/02/2023**		**ppts**	
	Instruction set-Data Transfer Instructions, String Instructions, Logical Instructions	**1**	**06/02/2023**		**ppts**	
	, Arithmetic Instructions, Transfer of Control Instructions, Processor Control Instructions	**1**	**07/02/2023**		**ppts**	
	Assembler Directives and Assembly Language Programming, Macros, Procedures	**1**	**08/02/2023**			**Assignment 2 & Quiz 1**
3.	**Memory and Peripherals interfacing**					
	Memory Interfacing - RAM and ROM Decoding Techniques – Partial and Absolute	**1**	**13/02/2023**		**ppts**	
	Design problems	**1**	**14/02/2023**		**ppts**	
	Design problems	**1**	**15/02/2023**		**ppts**	
	Design problems	**1**	**20/02/2023**		**ppts**	
	8255-PPI-Block diagram, CWR,	**1**	**21/02/2023**		**ppts**	
	8255 operating modes- Mode 0	**1**	**21/02/2023**		**ppts**	
	8255 interfacing with 8086.	**1**	**22/02/2023**		**ppts**	

	8255 Mode 2	**1**	**22/02/2023**		**ppts**	**TPS Activity**
	Unit Test-1		**28/2/23 to 3/3/23**			
	8257-DMAC-Block diagram, DMA operations and transfer modes.	**1**	**18/03/2023 (online)**		**ppts**	
	Programmable Interrupt Controller 8259-Block Diagram, Interfacing the 8259 in single and cascaded mode.	**1**	**01/04/2023 (online)**		**ppts**	**Assignment 3**
4.	**Intel 80386DX Processor**					
	Architecture of 80386 microprocessor	**1**	**08/03/2023**		**ppts**	**Quiz 2**
	80386 registers – General purpose Registers, EFLAGS and Control registers	**1**	**13/03/2023**		**ppts**	
	Real mode, Protected mode, virtual 8086 mode	**1**	**14/03/2023**		**ppts**	
	80386 memory management in Protected Mode – Descriptors and selectors, descriptor tables, the memory paging mechanism	**1**	**15/03/2023**		**ppts**	
	80386 memory management in Protected Mode – Descriptors and selectors, descriptor tables, the memory paging mechanism	**1**	**20/03/2023**		**Ppts, Videos links**	
	80386 memory management in Protected Mode – Descriptors and selectors, descriptor tables, the memory paging mechanism	**1**	**21/03/2023**		**ppts**	
5.	**Pentium Processor**					
	Pentium Architecture	**1**	**27/03/2023**		**ppts**	
	Superscalar Operation,	**1**	**27/03/2023**		**ppts**	
	Integer &Floating-Point Pipeline Stages,	**1**	**03/04/2023**		**ppts**	
	Branch Prediction Logic,	**1**	**05/04/2023**		**ppts**	
	Branch Prediction Logic,	**1**	**10/04/2023**		**ppts**	
	Cache Organization	**1**	**03/04/2023**		**Ppts, Videos links**	
	MESI protocol	**1**	**11/04/2023**		**Ppts, Videos links**	**Quiz 3**
6.	**Pentium 4**					

	Comparative study of 8086, 80386, Pentium I, Pentium II and Pentium III	**1**	**12/04/2023**		**ppts**	
	Pentium 4: Net burst micro architecture.	**1**	**12/04/2023**		**ppts**	
	Hyper threading technology and its use in Pentium 4	**1**	**15/04/2023 (online)**		**ppts**	

Textbooks:	
1	John Uffenbeck, "8086/8088 family: Design Programming and Interfacing", PHI.
2	Yu-Cheng Liu, Glenn A. Gibson, "Microcomputer System: The 8086/8088 Family,Architecture, Programming and Design", Prentice Hall
3	Walter A.Triebel, "The 80386DX Microprocessor: hardware, Software and Interfacing", Prentice Hall
4	Tom Shanley and Don Anderson, "Pentium Processor System Architecture", Addison-Wesley.
5	K. M. Bhurchandani and A. K. Ray, "Advanced Microprocessors and Peripherals", McGraw Hill
References:	
1	Barry B. Brey, "Intel Microprocessors", 8thEdition, Pearson Education India
2	Douglas Hall, "Microprocessor and Interfacing", Tata McGraw Hill.
3	Intel Manual
4	Peter Abel, "IBM PC Assembly language and Programming", 5th Edition, PHI
5	James Antonakons, "The Pentium Microprocessor", Pearson Education

Assessment:
Internal Assessment Test:
Assessment consists of two class tests of 20 marks each. The first class test is to be conducted when approx. 40% syllabus is completed and second class test when additional 40% syllabus is completed. Duration of each test shall be one hour.
End Semester Theory Examination:
1 Question paper will comprise of 6 questions, each carrying 20 marks.
2 The students need to solve total 4 questions.
3 Question No.1 will be compulsory and based on entire syllabus.
4 Remaining question (Q.2 to Q.6) will be selected from all the modules.

Useful Links	
1	https://swayam.gov.in/nd1_noc20_ee11/preview

2	https://nptel.ac.in/courses/108/105/108105102/
3	https://www.classcentral.com/course/swayam-microprocessors-and-microcontrollers-9894
4	https://www.mooc-list.com/tags/microprocessors

Evaluation Scheme
CIE Scheme
Internal Assessment: 20 (Average of two tests)

Internal Assessment Scheme

Module		Lecture Hours	No. of questions in			No. of questions in SEE
			Test 1	Test 2	Test 3*	
1	**The Intel Microprocessors 8086 Architecture**	8	02 (5 marks)	-	--	
2	**Instruction Set and Programming**	6	01 (5 Marks)	-	--	
3	**Memory and Peripherals interfacing.**	8	01 (5 Marks)	-	--	
4	**Intel 80386DX Processor**	7		02 (5 Marks)	--	
5	**Pentium Processor**	6	-	1 (5 Marks)	--	
6	**Pentium 4**	4	-	1 (5 Marks)	--	

Note: Four to six questions will be set in the Test paper

Verified by:

Programme Coordinator Subject Expert